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(54) ORGANIC EL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

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(57) ABSTRACT

A display device includes an underlying layer formed over a substrate; an insulating layer formed over the substrate to expose the underlying layer; and an organic EL layer formed on the exposed portion of the underlying layer, wherein a thickness of the insulating layer is formed to a predetermined thickness to prevent defects in the organic EL layer that can occur in an edge portion of the exposed portion.

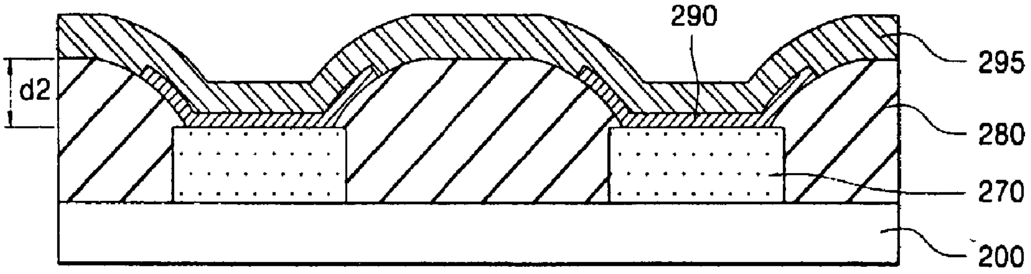


FIG. 1
(PRIOR ART)

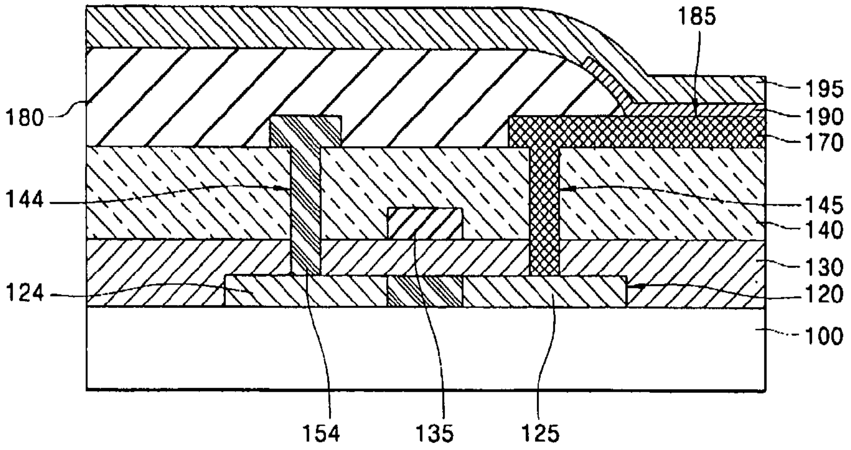


FIG. 2

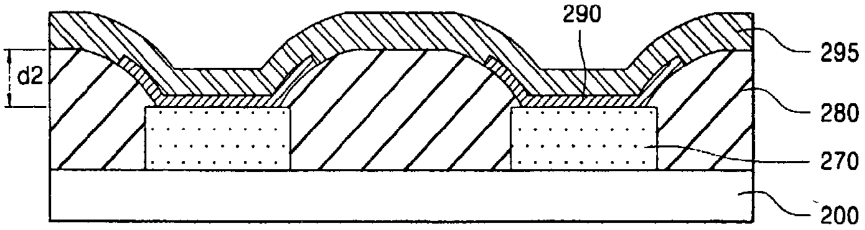


FIG. 3

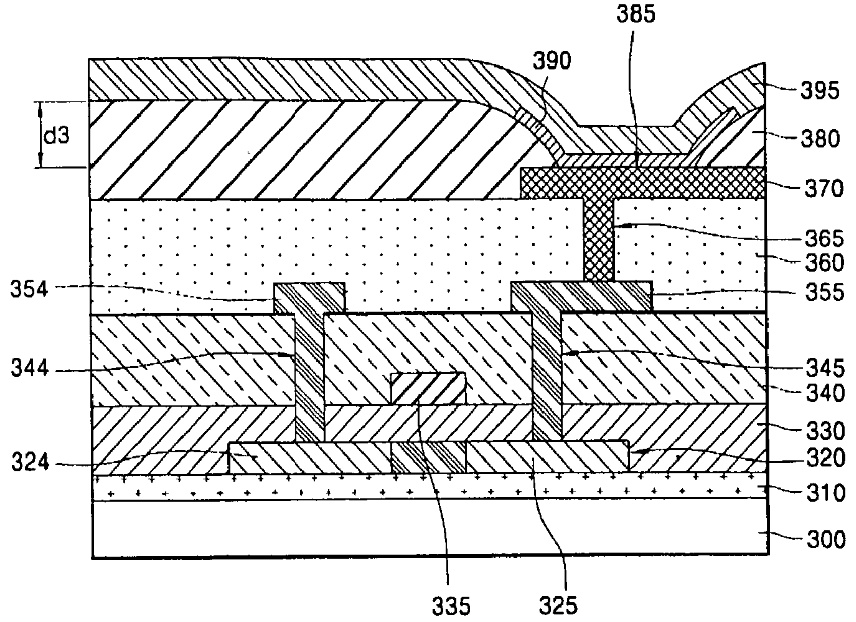

385
390
395
380
d3
370
365
360
354
355
344
345
340
330
324
320
310
300
335
325

FIG. 4

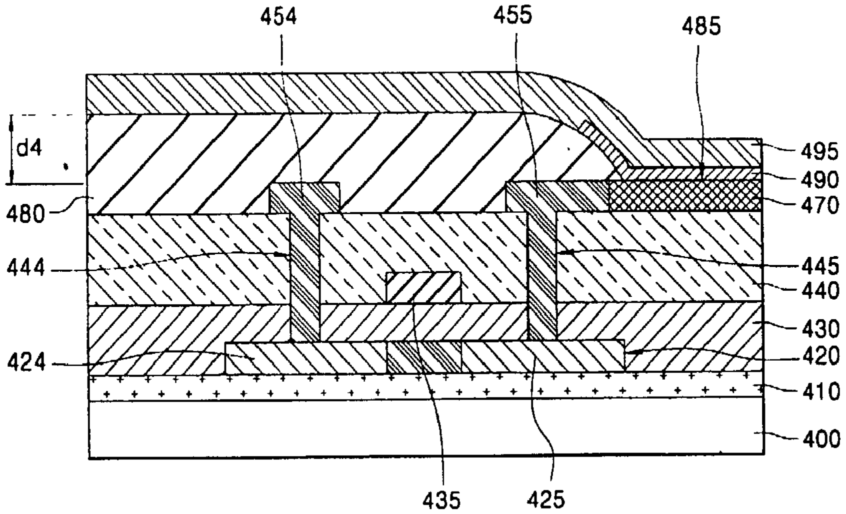

454
455
485
d4
495
490
470
480
444
445
440
430
424
420
410
400
435
425

FIG. 5

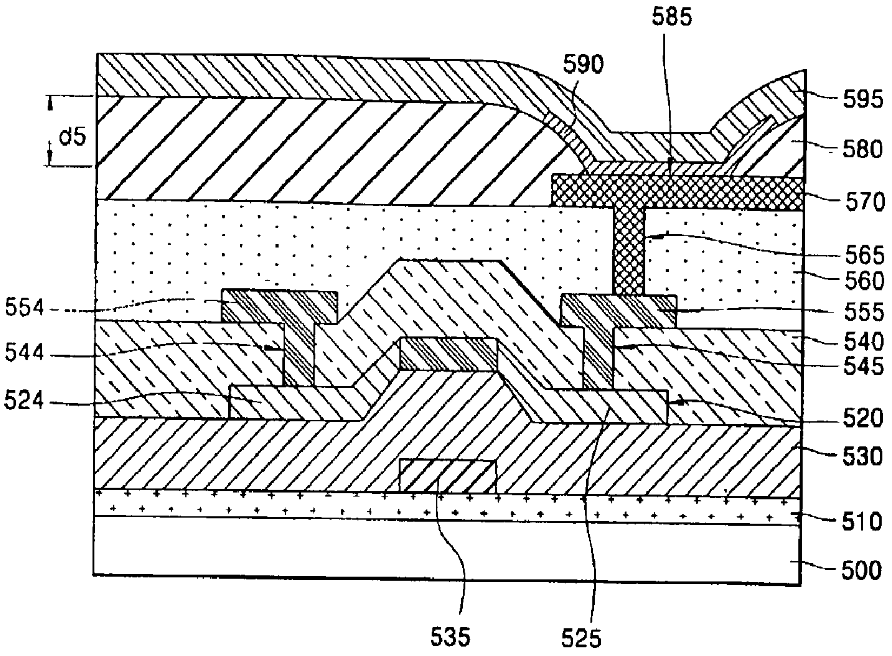

585
590
595
d5
580
570
565
560
554
555
540
544
545
524
520
530
510
500
535
525

FIG. 6

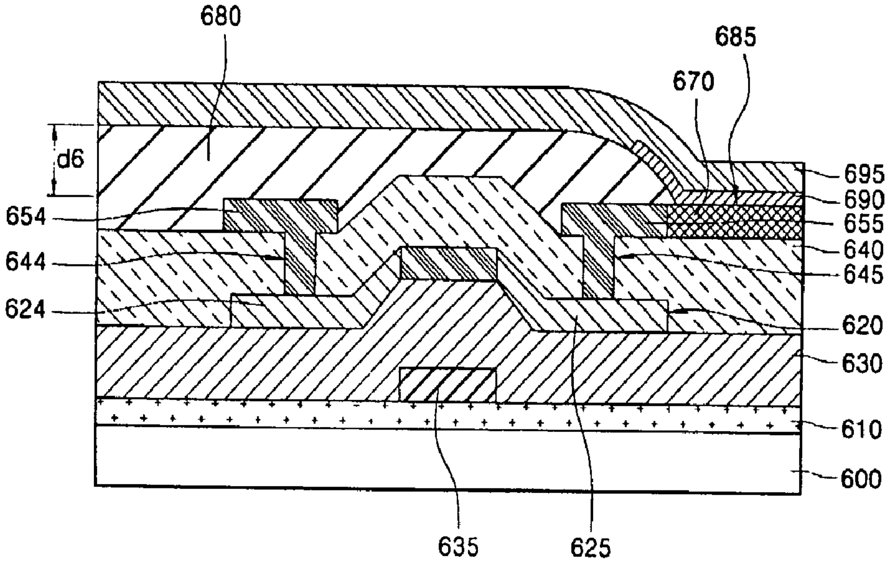

680
685
670
d6
695
690
654
655
640
644
645
624
620
630
610
600
635
625

FIG. 7A

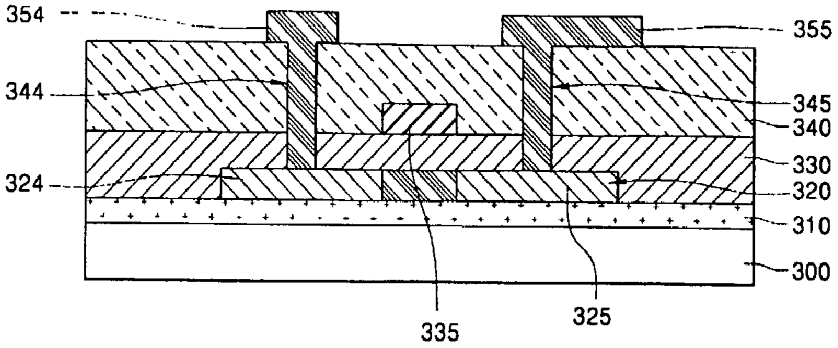
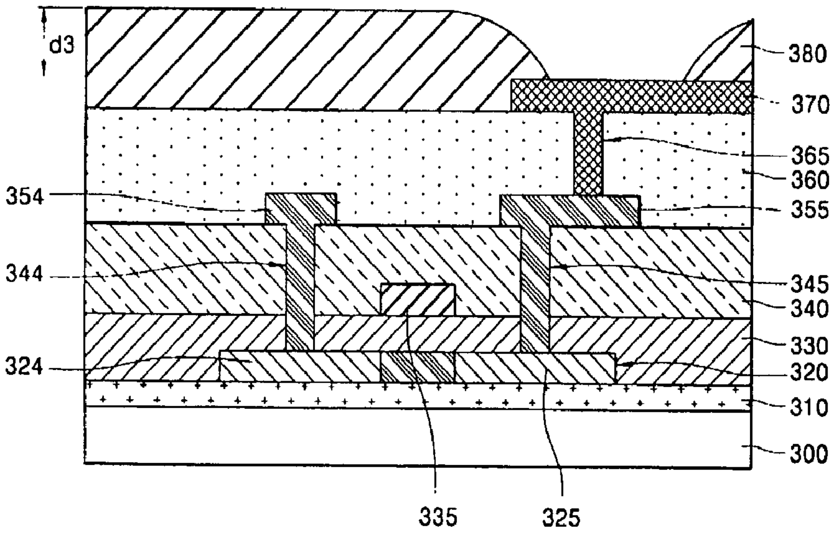

354
355
344
345
340
330
324
320
310
300
335
325

FIG. 7B


d3
380
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360
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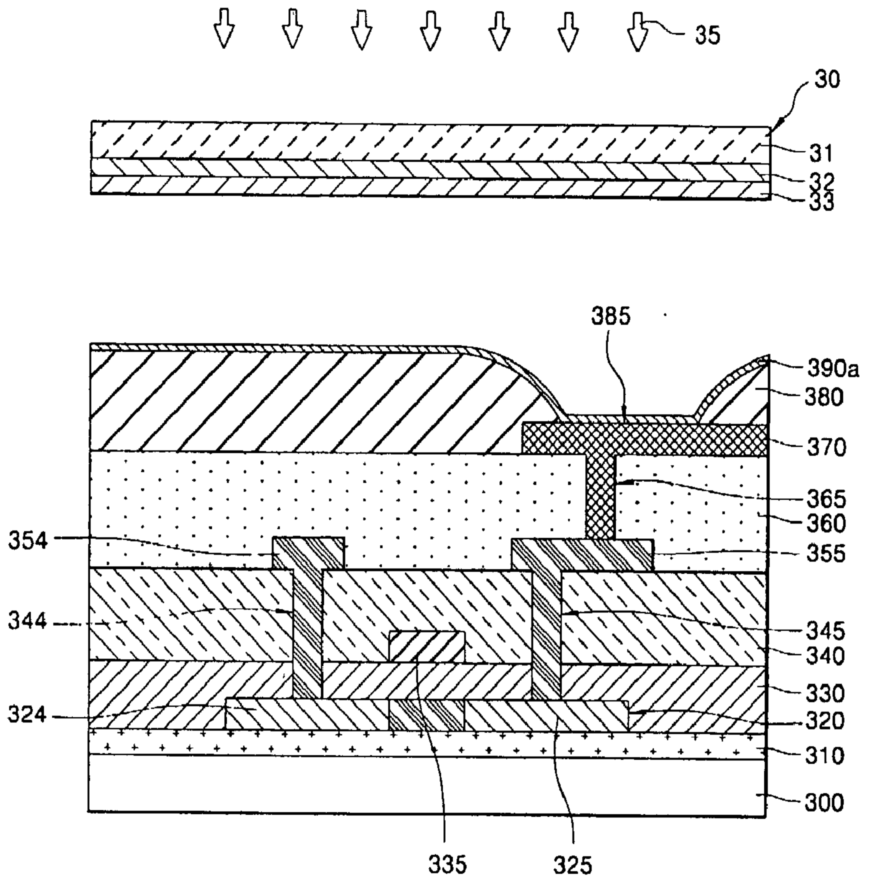
355
344
345
340
330
324
320
310
300
335
325

FIG. 7C


35
30
31
32
33
385
390a
380
370
365
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344
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330
324
320
310
300
335
325

FIG. 7D

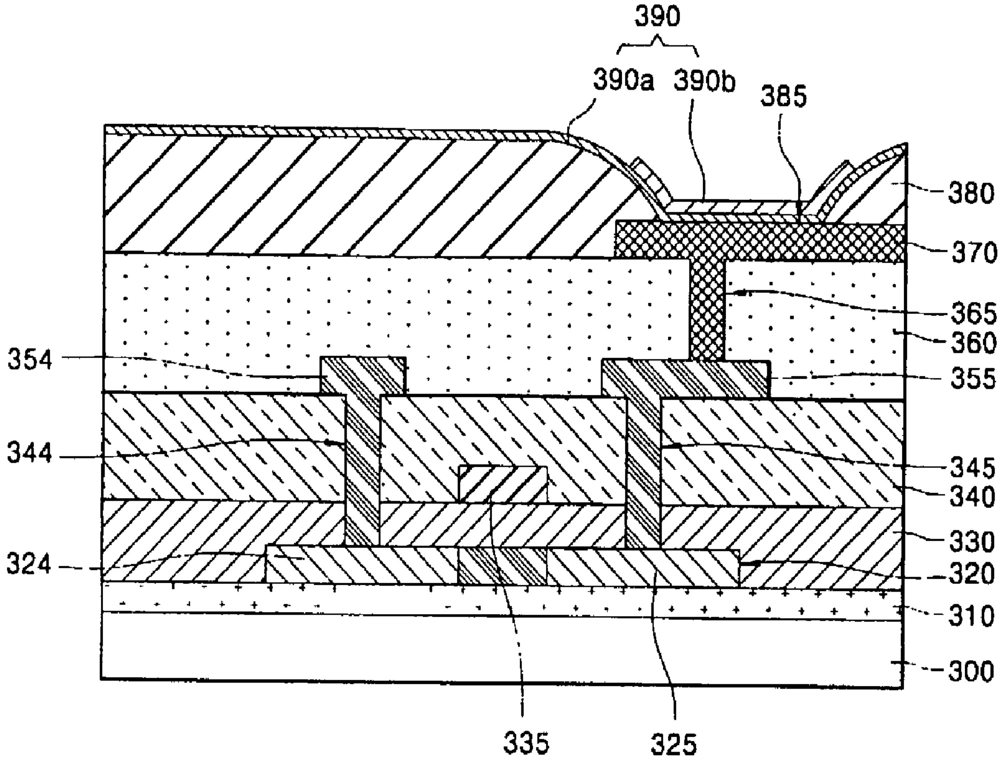

390
390a
390b
385
380
370
365
360
354
355
344
345
340
330
324
320
310
300
335
325

FIG. 8A

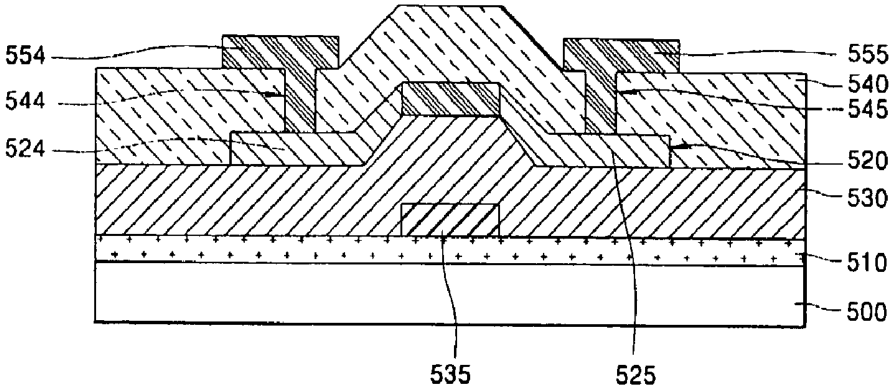

554
544
524
555
540
545
520
530
510
500
535
525

FIG. 8B

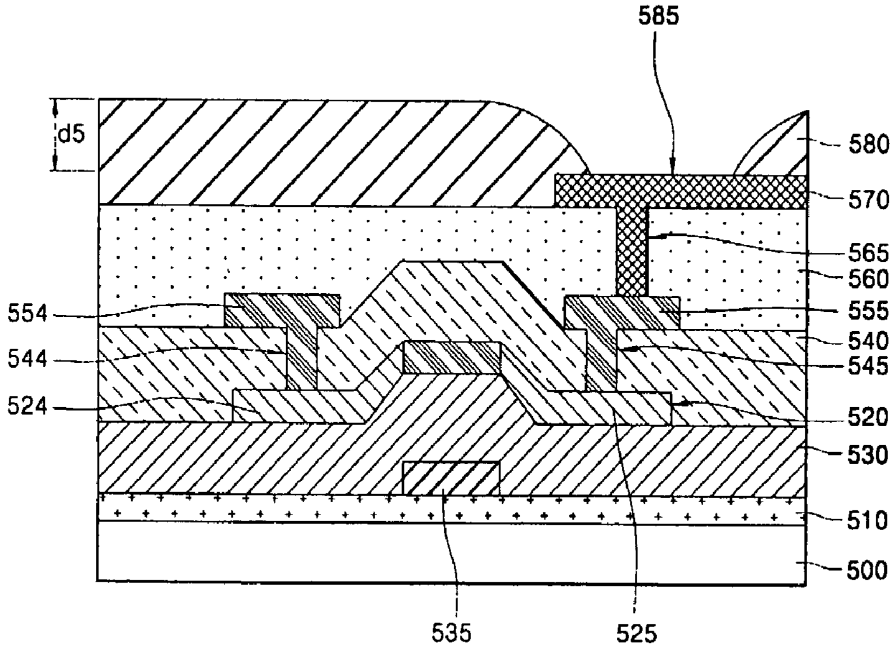
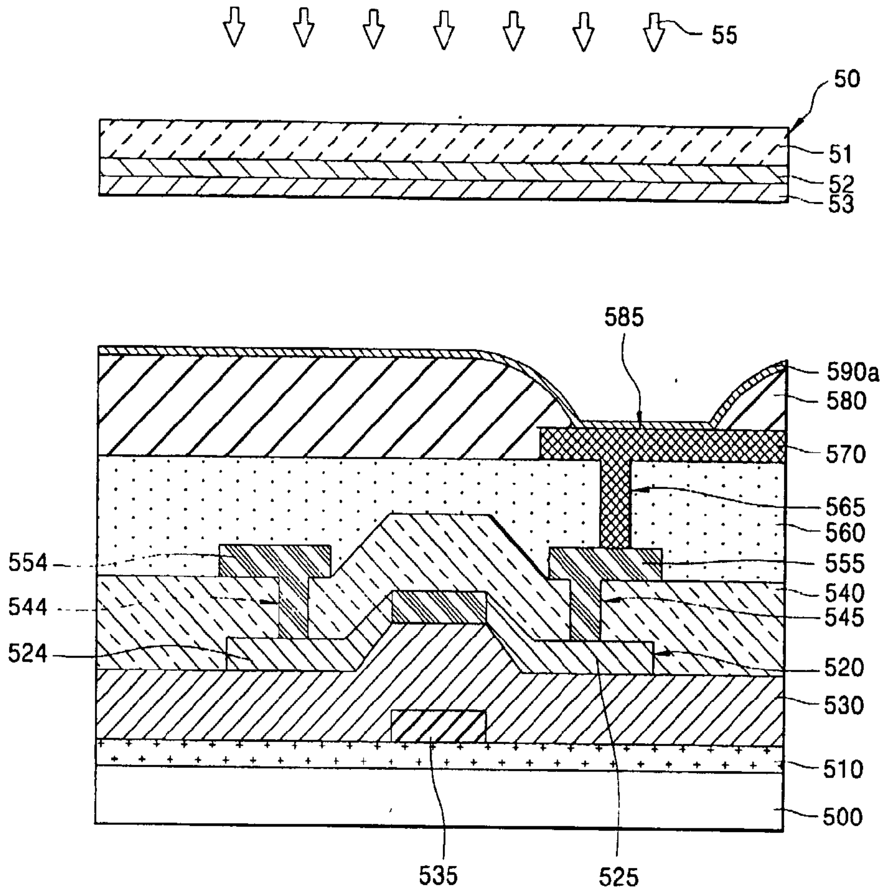

585
d5
580
570
565
560
554
555
540
544
545
524
520
530
510
500
535
525

FIG. 8C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50
51
52
53
585
590a
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570
565
560
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540
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520
530
510
500
535
525

FIG. 8D

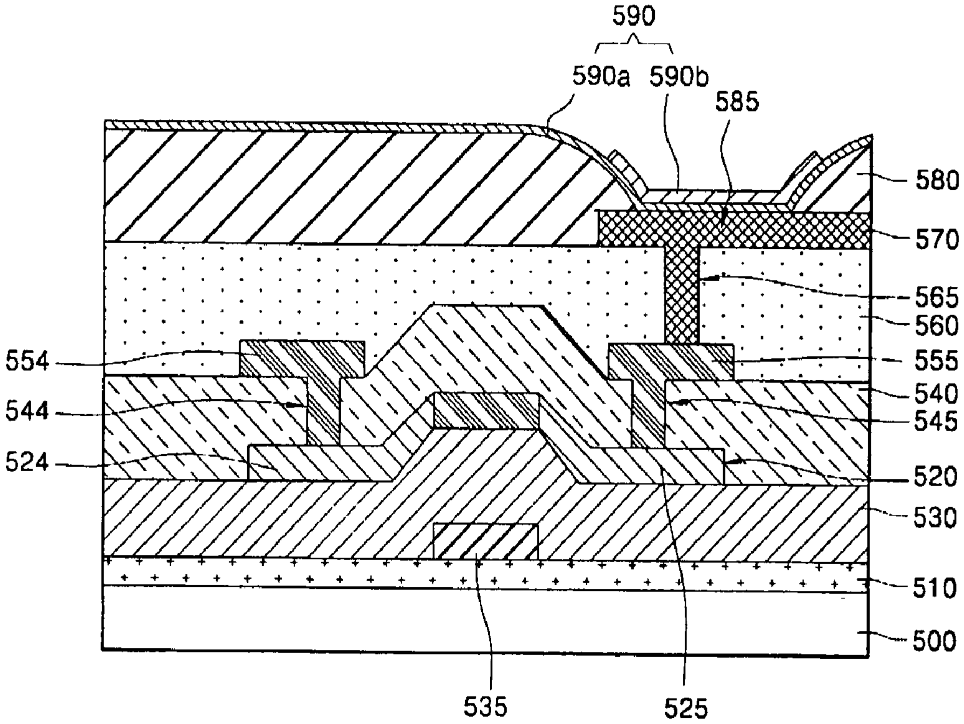

590
590a
590b
585
580
570
565
560
554
555
540
544
545
524
520
530
510
500
535
525

FIG. 9

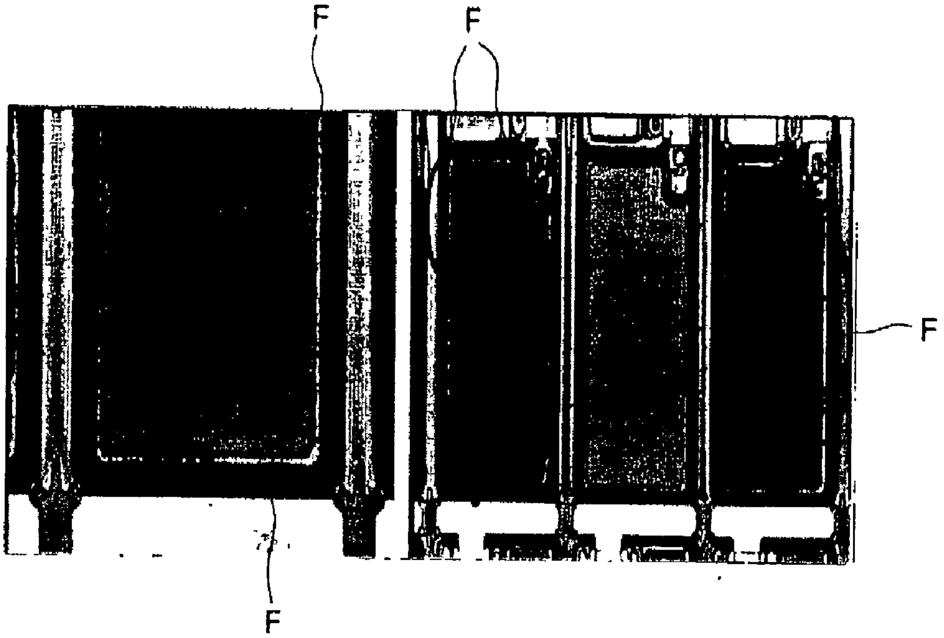
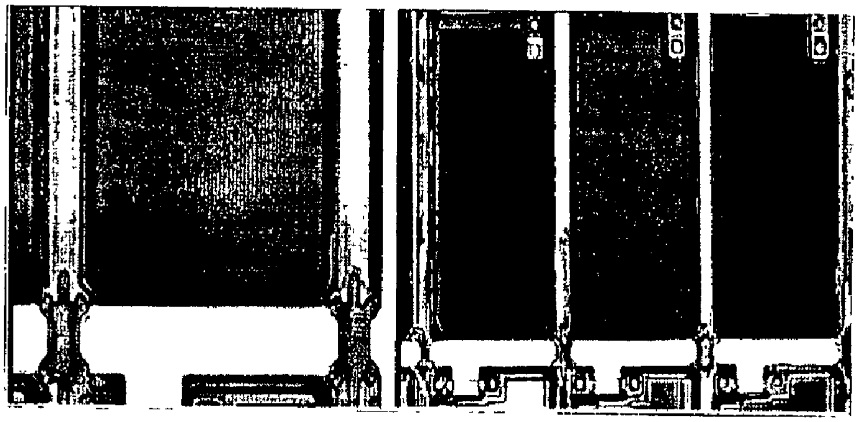


FIG. 10



ORGANIC EL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

CROSS-REFERENCE TO THE RELATED APPLICATIONS

[0001] This application claims the benefit of Korean Application No. 2001-73822 filed Nov. 26, 2001 in the Korean Industrial Property Office, the disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the invention

[0003] The present invention relates to a full color organic EL display device and a method of manufacturing the same.

[0004] 2. Description of Related Art

[0005] A full color organic EL display device includes an anode electrode, a hole injection layer, a hole transport layer, an organic EL layer having R, G and B color patterns, an electron transport layer, an electron injection layer, and a cathode electrode, which are sequentially stacked on an insulating substrate.

[0006] Of these, the organic EL layer is formed by using a vacuum deposition technique or a light etching technique using a shadow mask.

[0007] However, the vacuum deposition technique has a disadvantage in that there is a limitation on a minimum value of a physical gap and a large-sized organic EL display device, and it cannot be applied to an organic EL display device having fine patterns of tens of micrometers (μm) due to, for example, a mask transformation.

[0008] The light etching technique also has a disadvantage in that the organic EL layer can deteriorate due to a developing solution and etchant even though it can form fine patterns.

[0009] In order to overcome the above problems, a method of forming the organic EL layer using a thermal transfer technique is introduced. The thermal transfer technique is one which transfers a color pattern of the transfer film onto a substrate using a heat energy generated by light emitted from a light source.

[0010] Such a thermal transfer technique includes two techniques. One is related to controlling the light source, and the other is related to a configuration of the transfer film.

[0011] A laser beam is mainly used as a light source. A pigment colorant of the transfer film is scanned by the laser beam according to a desired pattern and transferred to the substrate, thereby forming a color pattern on the substrate.

[0012] U.S. Pat. No. 5,521,035 discloses methods of preparing color filter elements using laser induced transfer of colorants, wherein a Nd:YAG laser is used as a light source. The Nd:YAG laser forms a gaussian shaped beam having a Gauss distribution. The gaussian shaped beam, for example, having a diameter of more than 60 micrometers (μm), shows a characteristic that an energy distribution is gentler as it becomes more distant from a central point thereof. When the color pattern is formed using the gaussian shaped beam having a predetermined diameter, an intensity of the laser beam at an edge of the color pattern becomes weak. Consequently, the edge of the color pattern transferred is not clear and has a bad quality.

[0013] Techniques for a configuration of the transfer film are disclosed in U.S. Pat. No. 5,220,348 of D'Aurelio et al., U.S. Pat. No. 5,256,506 of Ellis et al., U.S. Pat. No. 5,278,023 of Bills et al., U.S. Pat. No. 5,308,737 of Bills et al., U.S. Pat. No. 5,998,085 of Isberg et al, U.S. Pat. No. 6,228,555 of Hoffend et al, U.S. Pat. Nos. 6,194,119 and 6,140,009 of Wolk et al., U.S. Pat. No. 6,057,067 of Isberg et al, U.S. Pat. No. 6,284,425 of Staral et al., U.S. Pat. Nos. 6,270,934, 6,190,826, and 5,981,136 of Jeffrey et al.

[0014] The techniques for a configuration of the transfer film are focused on a thermal transfer donor element which includes a base layer, a radiation absorber, a transfer layer and a gas-generating polymer layer. So, the techniques for a configuration of the transfer film do not suggest an improvement on reducing a deterioration of the edge portion of the color pattern.

[0015] Meanwhile, a conventional full color organic EL display device is manufactured such that a transparent electrode made of, for example, indium tin oxide (ITO), is formed over a thin film transistor (TFT) array substrate, and an insulating layer is formed over the whole surface of the substrate to expose a portion of the transparent electrode, and finally an organic EL layer is formed on the exposed portion of the transparent electrode.

[0016] An edge portion of the transparent electrode is covered with the insulating layer. This prevents a deterioration of the organic EL layer to increase a life span of the low molecular organic EL display device, and forms a wall to prevent a leakage of a solution during an ink-jet printing process to form the organic EL layer in the high molecular organic EL device. The technique is disclosed in EP 969701, SID 99 Digest P.396, IEEE '99 P. 107, and other similar documents.

[0017] Meanwhile, methods of manufacturing the full color organic EL display device using a laser transfer (i.e., thermal transfer) technique are disclosed in Korean Patent no. 10-0195175, Korean Patent Application no. 2000-49287, and U.S. Pat. No. 5,998,085. The transfer film is in contact with the TFT array substrate, and is scanned using a laser beam. The laser beam is absorbed into a light absorber of the transfer film and so is converted into a heat energy. An organic electroluminescent material is transferred from the transfer film to the substrate by the heat energy to thereby form a color pattern of the organic EL layer.

[0018] In the conventional art, a thickness of the insulating layer is set from 500 nm to 1000 nm or more than 1000 nm in consideration of a parastics capacitance. Due to the thick thickness of the insulating layer, defects in the edge of the organic thin layer occur in the case that the organic EL layer is formed using the laser transfer technique.

[0019] These defects can result from a characteristic of an underlying layer formed under the organic EL layer. For example, the defects occur when the underlying layer is formed non-uniformly, when the organic EL layer is not formed on the edge portion of the insulating layer to form a hole, or when the underlying layer is separated from other layers.

[**0020**] U.S. Pat. No. 5,684,365 discloses a method of preventing defects of the organic EL layer which can occur in a boundary between the transparent electrode and the insulating layer.

[**0021**] **FIG. 1** is a cross-sectional view illustrating an organic EL display device shown in U.S. Pat. No. 5,648,365. Referring to **FIG. 1, a** semiconductor layer **120** is formed on an insulating substrate **100** in the form of an island. The semiconductor layer **120** includes source and drain regions **124** and **125**, respectively, and is made of poly silicon. A gate insulating layer **130** is formed over the whole surface of the insulating substrate **100** and covers the semiconductor layer **120**. A gate electrode **135** is formed on the gate insulating layer **130**. An interlayer insulating layer **140** is formed on the gate insulating layer **130** and covers the gate electrode **135**. Contact holes **144** and **145** are formed to expose a portion of the source region **124** and a portion of the drain region **125**, respectively. A source electrode **154** is electrically connected to the source region **124** via the contact hole **144**. A pixel electrode **170** is electrically connected to the drain region **125** via the contact hole **145**. A passivation layer **180** is formed over the whole surface of the insulating substrate **100** to expose a portion of the pixel electrode **170**, thereby forming an opening portion **185**. An organic EL layer **190** is formed on the exposed portion of the pixel electrode **170** through the opening portion **185**. A cathode electrode **195** is formed to cover the organic EL layer **190**.

[**0022**] An edge of the passivation layer **180** defining the opening portion **185** has a taper angle of 10° to 30°. The tapered edge of the passivation layer **180** serves to improve an adhesion of the organic EL layer **190**, thereby preventing defects of the organic EL layer **190**.

[**0023**] However, in the case of forming the organic EL layer using the laser transfer technique, there are still problems in that the defects in the edge of the organic thin layer occur when the thickness of the insulating layer is more than 500 nm, even though the insulating layer is formed in order to form a taper angle in the edge of the passivation layer.

SUMMARY OF THE INVENTION

[**0024**] Accordingly, it is an object of the present invention to provide an organic EL display device and a method of manufacturing the same, which can prevent defects of an organic EL layer which can occur in an edge portion of an opening portion.

[**0025**] Additional objects and advantages of the invention will be set forth in part in the description which follows and, in part, will be obvious from the description, or may be learned by practice of the invention.

[**0026**] The foregoing and other objects of the present invention are achieved by providing a display device comprising: an underlying layer formed over a substrate; an insulating layer formed over the substrate to expose the underlying layer; and an organic EL layer formed on the exposed portion of the underlying layer, wherein a thickness of the insulating layer is less than 500 nm.

[**0027**] The foregoing and other objects of the present invention may also be achieved by providing an organic EL display device comprising: a thin film transistor having source and drain electrodes formed over a substrate; a lower electrode contacting one of the source and drain electrodes of the thin film transistor; an insulating layer formed over the substrate to expose the lower electrode; and an organic EL layer formed on the exposed portion of the lower electrode, wherein a thickness of the insulating layer is less than 500 nm.

[**0028**] The foregoing and other objects of the present invention may also be achieved by providing a method of manufacturing a display device comprising: forming an underlying layer over a substrate; forming an insulating layer over a substrate to expose the underlying layer; and forming an organic EL layer on the exposed portion of the underlying layer, wherein a thickness of the insulating layer is less than 500 nm.

[**0029**] The method further comprises forming a thin film transisor having source and drain electrodes over the substrate before the forming of the underlying layer. The underlying layer is a lower electrode connecting one of the source and drain electrodes of the thin film transisor. The organic EL layer is formed using a laser tranfer technique.

[**0030**] In an embodiment of the present invention, the thickness of the insulating layer is less than 200 nm. In an alternative embodiment, the thickness of the insulating layer is in a range between 10 nm and 500 nm. In yet another alternative embodiment, the thickness of the insulating layer is in a range between 100 nm and 200 nm.

[**0031**] The insulating layer is formed to cover an edge of the underlying layer. A portion of the insulating layer corresponding to the edge of the underlying layer has a thickness of less than 200 nm. A portion of the insulating layer corresponding to an edge of the underlying layer has a thickness of 10 nm to 500 nm. The portion of the insulating layer corresponding to the edge of the underlying layer has a thickness of 100 nm to 200 nm.

[**0032**] In an aspect of the present invention, a step from the insulating layer to the underlying layer is less than 200 nm. In another aspect of the invention, a step from the insulating layer to the underlying layer is in a range between 10 nm to 500 nm. More specifically, the step from the insulating layer to the underlying layer is in a range between 100 nm to 200 nm.

BRIEF DESCRIPTION OF THE DRAWINGS

[**0033**] These and other objects and advantages of the invention will become apparent and more readily appreciated from the following description of the embodiments, taken in conjunction with the accompanying drawings of which:

[**0034**] **FIG. 1** is a cross-sectional view illustrating a conventional organic EL display device;

[**0035**] **FIG. 2** is a cross-sectional view illustrating a passive matrix organic EL display device according to an embodiment of the present invention;

[**0036**] **FIG. 3** is a cross-sectional view illustrating a top-gate type thin film transistor (TFT) organic EL display device according to another embodiment of the present invention;

[**0037**] **FIG. 4** is a cross-sectional view illustrating a top-gate type TFT organic EL display device according to yet another embodiment of the present invention;

[0038] **FIG. 5** is a cross-sectional view illustrating a bottom-gate type TFT organic EL display device according to yet another embodiment of the present invention;

[0039] **FIG. 6** is a cross-sectional view illustrating a bottom-gate type TFT organic EL display device according to yet another embodiment of the present invention;

[0040] **FIGS. 7A** to **7D** are cross-sectional views illustrating a process of manufacturing the organic EL display device of **FIG. 3**;

[0041] **FIGS. 8A** to **8D** are cross-sectional views illustrating a process of manufacturing the organic EL display device of **FIG. 5**;

[0042] **FIG. 9** is a photograph illustrating the organic EL layer of the conventional organic EL display device; and

[0043] **FIG. 10** is a photograph illustrating the organic EL layer of the organic display device according to an embodiment of the present invention.

DETAILED DESCRIPTION OF PREFFERED EMBODIMENTS

[0044] Reference will now be made in detail to the embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to like elements throughout. The embodiments are described below in order to explain the present invention by referring to the figures.

[0045] Though the present invention reduces a thickness of the insulating layer as less than 500 nm and an organic EL display device of the present invention don't have defect due to a parastics capacitance, thereby a transfer characteristics of the present invention can be improved.

[0046] **FIG. 2** is a cross-sectional view illustrating a passive matrix organic EL display device according to an embodiment of the present invention.

[0047] An anode electrode **270** is formed on an insulating substrate **200**. The anode electrode **270** also serves as a pixel electrode and is made of a transparent conductive material such as indium tin oxide (ITO) and indium zinc oxide (IZO). An insulating layer **280** is formed to cover an edge of the pixel electrode **270**. An organic EL layer **290** is formed on the pixel electrode **270**. A cathode electrode **295** is formed on the insulating layer **280** and covers the organic EL layer **290**.

[0048] The organic EL layer **290** includes a hole injection layer, a hole transport layer, a light-emitting layer having R, G and B color patterns, an electron transport layer, and an electron injection layer, which are sequentially stacked.

[0049] The insulating layer **280** has a thickness of less than 500 nm and preferably 10 nm to 500 nm. A thickness d2 of a portion of the insulating layer **280** corresponding to an edge portion of the pixel electrode **270** is less than 500 nm, preferably 10 nm to 500 nm, and more preferably 100 nm to 200 nm.

[0050] When the organic EL layer **290** is formed to cover an edge portion of the insulating layer **280** having a thickness described above, edge defects of the organic EL layer **290** do not occur in a boundary between the pixel electrode **270** and the insulating layer **280**, as shown in **FIG. 10**.

[0051] **FIG. 3** is a cross-sectional view illustrating a top-gate type thin film transistor (TFT) organic EL display device according to another embodiment of the present invention.

[0052] A buffer layer **310** is formed on an insulating substrate **300**. A semiconductor layer **320** is formed on the buffer layer **310**. The semiconductor layer **320** includes source and drain regions **324** and **325**, respectively. A gate insulating layer **330** is formed over the whole surface of the insulating substrate **300** and covers the semiconductor layer **320**. A gate electrode **335** is formed on the gate insulating layer **330**. An interlayer insulating layer **340** is formed over the whole surface of the insulating substrate **300** and covers the gate electrode **335**. Contact holes **344** and **345** are formed to expose a portion of the source region **324** and a portion of the drain region **325**, respectively. Source and drain electrodes **354** and **355** are electrically connected to the source and the drain regions **324** and **325** through the contact holes **344** and **345**, respectively.

[0053] A passivation layer **360** is formed over the whole surface of the insulating substrate **300**. A via hole **365** is formed to expose either the source or the drain electrodes **354** and **355**. In **FIG. 3**, the via hole **365** exposes a portion of the drain electrode **355**. A pixel electrode **370** is formed on the passivation layer **360** and is electrically connected to the drain electrode **355** through the via hole **365**. The pixel electrode **370** serves as an anode electrode.

[0054] A planarization layer **380** is formed on the passivation layer **360** and covers an edge portion of the pixel electrode **370** to expose a portion of the pixel electrode **370**, thereby forming an opening portion **385** on the pixel electrode **370**. An organic EL layer **390** is formed on the exposed portion of the pixel electrode **370** and covers an edge portion of the planarization layer **380**. A cathode electrode **395** is formed on the planarization layer **380** and covers the organic EL layer **390**.

[0055] The organic EL layer **390** includes a hole injection layer, a hole transport layer, a light-emitting layer having R, G and B color patterns, an electron transport layer, and an electron injection layer, which are sequentially stacked.

[0056] The planarization layer **380** has a thickness of less than 500 nm and preferably 10 nm to 500 nm. A thickness d3 of a portion of the insulating layer **380** corresponding to an edge portion of the pixel electrode **370** is less than 500 nm, preferably 10 nm to 500 nm, and more preferably 100 nm to 200 nm.

[0057] When the organic EL layer **390** is formed to cover an edge portion of the insulating layer **380** having a thickness described above, edge defects of the organic EL layer **390** do not occur in a boundary between the pixel electrode **370** and the insulating layer **380**, as shown in **FIG. 10**.

[0058] **FIG. 4** is a cross-sectional view illustrating a top-gate type TFT organic EL display device according to another embodiment of the present invention.

[0059] A buffer layer **410** is formed on an insulating substrate **400**. A semiconductor layer **420** is formed on the buffer layer **410**. The semiconductor layer **420** includes source and drain regions **424** and **425**, respectively. A gate insulating layer **430** is formed over the whole surface of the insulating substrate **400** and covers the semiconductor layer

420. A gate electrode **435** is formed on the gate insulating layer **430**. An interlayer insulating layer **440** is formed over the whole surface of the insulating substrate **400** and covers the gate electrode **435**. Contact holes **444** and **445** are formed to expose a portion of the source region **424** and a portion of the drain region **425**, respectively. Source and drain electrodes **454** and **455** are electrically connected to the source and the drain regions **424** and **425** through the contact holes **444** and **445**, respectively.

[0060] A pixel electrode **470** is formed on the interlayer insulating layer **440** and is electrically connected to either of the source and the drain electrodes **454** and **455**. In **FIG. 4**, the pixel electrode **470** is electrically to the drain electrode **455**. The pixel electrode **470** serves as an anode electrode.

[0061] An insulating layer **480** is formed on the interlayer insulating layer **440** and covers an edge portion of the pixel electrode **470** to expose a portion of the pixel electrode **470**, thereby forming an opening portion **485** on the pixel electrode **470**. The insulating layer **480** is a passivation layer or a planarization layer.

[0062] An organic EL layer **490** is formed on the exposed portion of the pixel electrode **470** and covers an edge portion of the planarization layer **480**. A cathode electrode **495** is formed on the insulating layer **480** and covers the organic EL layer **490**.

[0063] The organic EL layer **490** includes a hole injection layer, a hole transport layer, a light-emitting layer having R, G and B color patterns, an electron transport layer, and an electron injection layer, which are sequentially stacked.

[0064] The insulating layer **480** has a thickness of less than 500 nm and preferably 10 nm to 500 nm. A thickness d4 of a portion of the insulating layer **480** corresponding to an edge portion of the pixel electrode **470** is less than 500 nm, preferably 10 nm to 500 nm, and more preferably 100 nm to 200 nm.

[0065] When the organic EL layer **490** is formed to cover an edge portion of the insulating layer **480** having a thickness described above, edge defects of the organic EL layer **490** do not occur in a boundary between the pixel electrode **470** and the insulating layer **480** as shown in **FIG. 10**.

[0066] **FIG. 5** is a cross-sectional view illustrating a bottom-gate type TFT organic EL display device according to another embodiment of the present invention.

[0067] A buffer layer **510** is formed on an insulating substrate **500**. A gate electrode **535** is formed on the buffer layer **510**. A gate insulating layer **530** is formed over the whole surface of the insulating substrate **500** and covers the gate electrode **535**. A semiconductor layer **520** is formed on the gate insulating layer **530**. The semiconductor layer **520** includes source and drain regions **524** and **525**, respectively. An interlayer insulating layer **540** is formed over the whole surface of the insulating substrate **500** and covers the semiconductor layer **520**. Contact holes **544** and **545** are formed to expose a portion of the source region **524** and a portion of the drain region **525**, respectively. Source and drain electrodes **554** and **555** are electrically connected to the source and the drain regions **524** and **525** through the contact holes **544** and **545**, respectively.

[0068] A passivation layer **560** is formed over the whole surface of the insulating substrate **500**. A via hole **565** is formed to expose either the source or the drain electrodes **554** and **555**. In **FIG. 5**, the via hole **565** exposes a portion of the drain electrode **555**. A pixel electrode **570** is formed on the passivation layer **560** and is electrically connected to the drain electrode **555** through the via hole **565**. The pixel electrode **570** serves as an anode electrode.

[0069] A planarization layer **580** is formed on the passivation layer **560** and covers an edge portion of the pixel electrode **570** to expose a portion of the pixel electrode **570**, thereby forming an opening portion **585** on the pixel electrode **570**. An organic EL layer **590** is formed on the exposed portion of the pixel electrode **570** and covers an edge portion of the planarization layer **580**. A cathode electrode **595** is formed on the planarization layer **580** and covers the organic EL layer **590**.

[0070] The organic EL layer **590** includes a hole injection layer, a hole transport layer, a light-emitting layer having R, G and B color patterns, an electron transport layer, and an electron injection layer, which are sequentially stacked.

[0071] The planarization layer **580** has a thickness of less than 500 nm and preferably 10 nm to 500 nm. A thickness d5 of a portion of the insulating layer **580** corresponding to an edge portion of the pixel electrode **570** is less than 500 nm, preferably 10 nm to 500 nm, and more preferably 100 nm to 200 nm.

[0072] When the organic EL layer **590** is formed to cover an edge portion of the insulating layer **580** having a thickness described above, edge defects of the organic EL layer **590** do not occur in a boundary between the pixel electrode **570** and the insulating layer **380** as shown in **FIG. 10**.

[0073] **FIG. 6** is a cross-sectional view illustrating a bottom-gate type TFT organic EL display device according to another embodiment of the present invention.

[0074] A buffer layer **610** is formed on an insulating substrate **600**. A gate electrode **635** is formed on the buffer layer **610**. A gate insulating layer **630** is formed over the whole surface of the insulating substrate **600** and covers the gate electrode **635**. A semiconductor layer **620** is formed on the gate insulating layer **630**. The semiconductor layer **620** includes source and drain regions **624** and **625**, respectively. An interlayer insulating layer **640** is formed over the whole surface of the insulating substrate **600** and covers the semiconductor layer **620**. Contact holes **644** and **645** are formed to expose a portion of the source region **624** and a portion of the drain region **625**, respectively. Source and drain electrodes **654** and **655** are electrically connected to the source and the drain regions **624** and **625** through the contact holes **644** and **645**, respectively.

[0075] A pixel electrode **670** is formed on the interlayer insulating layer **640** and is electrically connected to either the source or the drain electrodes **654** and **655**. In **FIG. 6**, the pixel electrode **670** is electrically to the drain electrode **655**. The pixel electrode **670** serves as an anode electrode.

[0076] An insulating layer **680** is formed on the interlayer insulating layer **640** and covers an edge portion of the pixel electrode **670** to expose a portion of the pixel electrode **670**, thereby forming an opening portion **685** on the pixel electrode **670**. The insulating layer **680** is the passivation layer or the planarization layer.

[**0077**] An organic EL layer **690** is formed on the exposed portion of the pixel electrode **670** and covers an edge portion of the planarization layer **680**. A cathode electrode **695** is formed on the insulating layer **680** and covers the organic EL layer **690**.

[**0078**] The organic EL layer **690** includes a hole injection layer, a hole transport layer, a light-emitting layer having R, G and B color patterns, an electron transport layer, and an electron injection layer, which are sequentially stacked.

[**0079**] The insulating layer **680** has a thickness of less than 500 nm and preferably 10 nm to 500 nm. A thickness d**6** of a portion of the insulating layer **680** corresponding to an edge portion of the pixel electrode **670** is less than 500 nm, preferably 10 nm to 500 nm, and more preferably 100 nm to 200 nm.

[**0080**] When the organic EL layer **690** is formed to cover an edge portion of the insulating layer **680** having a thickness described above, edge defects of the organic EL layer **690** do not occur in a boundary between the pixel electrode **670** and the insulating layer **680**, as shown in **FIG. 10**.

[**0081**] As described above, the organic EL layer can be formed without any defects by defining a thickness of the insulating layer.

[**0082**] Methods of manufacturing the organic EL display device according to several embodiments of the present invention are described below.

[**0083**] **FIGS. 7A** to **7D** are cross-sectional views illustrating a process of manufacturing the organic EL display device of **FIG. 3**.

[**0084**] Referring to **FIG. 7A, a** buffer layer **310** is formed on an insulating substrate **300** after cleaning the insulating substrate **300**. The insulating substrate **300** is preferably made of glass, but not limited thereto. The buffer layer **310** is preferably made of SiO_2, but not limited thereto. A semiconductor layer **320** is formed on the buffer layer **310**. The semiconductor layer **320** is preferably made of a poly silicon, but not limited thereto. The semiconductor layer **320** can be formed by various methods. For example, an amorphous silicon layer is deposited on the buffer layer **310** and is annealed by using an excimer laser to form a poly silicon layer, and the poly silicon layer is patterned in the form of an island to thereby form the semiconductor layer **320**.

[**0085**] A gate insulating layer **330** is formed over the whole surface of the insulating substrate **300** and covers the semiconductor layer **320**. The gate insulating layer **330** is preferably made of SiO_2, but not limited thereto. A gate electrode **335** is formed on the gate insulating layer **330**. Using the gate electrode **335** as a mask, a p- or an n-type impurity is ion-doped into the semiconductor layer **320** to form source and drain regions **324** and **325**, respectively.

[**0086**] An interlayer insulating layer **340** is formed over the whole surface of the insulating substrate **300** and covers the gate electrode **335**. The interlayer insulating layer **340** is preferably made of SiNx, but not limited thereto. The gate insulating layer **330** and the interlayer insulating layer **340** are etched to form contact holes **344** and **345** to expose a portion of the source region **324** and a portion of the drain region **325**, respectively.

[**0087**] A metal layer is deposited on the interlayer insulating layer **340** and patterned into source and drain electrodes **354** and **355**, respectively. The source and the drain electrodes **354** and **355** are electrically connected to the source and the drain regions **324** and **325** through the contact holes **344** and **345**, respectively.

[**0088**] Referring to **FIG. 7B, a** passivation layer **360** is formed over the whole surface of the insulating substrate **300**. The passivation layer is preferably made of SiO_2, but not limited thereto. The passivation layer **360** is patterned to form a via hole **365**. The via hole **365** exposes either the source or the drain electrodes **354** and **355**. In **FIG. 7**B, the via hole **365** exposes a portion of the drain electrode **355**.

[**0089**] A transparent conductive layer is deposited on the passivation layer **360** to a thickness of 200 nm using a sputtering technique and dry-etched to form a pixel electrode **370** as an anode electrode. The pixel electrode **370** is preferably made of a transparent conductive material such as indium tin oxide (ITO) or indium zinc oxide (IZO). The pixel electrode **370** is electrically connected to the drain electrode **355** through the via hole **365**.

[**0090**] Subsequently, a planarization layer **380** is formed on the passivation layer **360** and covers an edge portion of the pixel electrode **370** to expose a portion of the pixel electrode **370**, thereby forming an opening portion **385** on the pixel electrode **370**. In other words, an insulating layer made of acryl is deposited on the passivation layer **360** to a thickness of 350 nm using a spin-coating technique at a speed of 3000 rpm and patterned to define the opening portion **385**. Thereafter, the insulating layer is baked at a temperature of 220° C., thereby forming the insulating layer **380** in which a taper angle of an edge portion thereof is **150** and a thickness d**3** of a portion of the insulating layer formed on an edge of the pixel electrode **370** is 250 nm.

[**0091**] Referring to **FIGS. 7C and 7D**, an organic EL layer **390** is formed on the exposed portion of the pixel electrode **370** to cover an edge portion of the planarization layer **380** using a laser transfer technique.

[**0092**] In more detail, a PEDOT is spin-coated to a thickness of 50 nm at a speed of 3000 rpm and heat-treated at a temperature of 200° C. during five minutes to thereby form a hole transport layer **390***a*. Subsequently, three pieces of transfer films are manufactured. For the sake of description convenience, a method of manufacturing one transfer film **30** for an R color pattern is described.

[**0093**] The transfer film **30** for the R color pattern is manufactured as follows: on a base film **31** having a transfer layer **32** formed thereon, an R color organic electroluminescent material is spin-coated to a thickness of 80 nm at a speed of 2000 rpm using a xylene solution having a concentration of 1.0 wt/V %.

[**0094**] After aligning the transfer film **30** with the array substrate, the transfer film **30** is scanned by an infrared-rays laser **35** so that a desired pattern is transferred to the hole transport layer **390***a,* thereby forming the R color pattern **390***b* of the organic EL layer.

[**0095**] In the same method, G and B color patterns are formed to complete the organic EL layer **390**. The organic EL layer **390** can further include a hole injection layer, an electron transport layer and an electron injection layer.

[**0096**] A cathode electrode **395** (see **FIG. 3**) is formed on the planarization layer **380** and covers the organic EL layer

390. Preferably, the cathode electrode **395** has a dual-layered structure of Ca/Ag. Preferably, the Ca layer and the Ag layer have a thickness of 30 nm and 270 nm, respectively.

[**0097**] Finally, an encapsulation process is performed to complete the organic EL display device according to the embodiments of the present invention.

[**0098**] **FIGS. 8A** to **8**D are cross-sectional views illustrating a process of manufacturing the organic EL display device of **FIG. 5**.

[**0099**] Referring to **FIG. 8A, a** buffer layer **510** is formed on an insulating substrate **500** after cleaning the insulating substrate **500**. The insulating substrate **500** is preferably made of glass, but not limited thereto. The buffer layer **510** is preferably made of SiO_2, but not limited thereto. A gate electrode **535** is formed on the buffer layer **510**. A gate insulating layer **530** is formed over the whole surface of the insulating substrate **500** and covers the gate electrode **535**.

[**0100**] A semiconductor layer **520** is formed on the gate insulating layer **530**. The semiconductor layer **520** is preferably made of a poly silicon, but not limited thereto. The semiconductor layer **520** can be formed by various methods. For example, an amorphous silicon layer is deposited on the gate insulating layer **530** and is annealed by using an excimer laser to form a poly silicon layer, and the poly silicon layer is patterned in the form of an island to thereby form the semiconductor layer **520**.

[**0101**] Using the gate electrode **535** as a mask, a p- or an n-type impurity is ion-doped into the semiconductor layer **520** to form source and drain regions **524** and **525**.

[**0102**] An interlayer insulating layer **540** is formed over the whole surface of the insulating substrate **500** and covers the gate electrode **535**. The interlayer insulating layer **540** is preferably made of SiNx, but not limited thereto. The gate insulating layer **530** and the interlayer insulating layer **540** are etched to form contact holes **544** and **545** to expose a portion of the source region **524** and a portion of the drain region **525**, respectively.

[**0103**] A metal layer is deposited on the interlayer insulating layer **540** and patterned into source and drain electrodes **554** and **555**, respectively. The source and the drain electrodes **554** and **555** are electrically connected to the source and the drain regions **524** and **525** through the contact holes **544** and **545**, respectively.

[**0104**] Referring to **FIG. 8B, a** passivation layer **560** is formed over the whole surface of the insulating substrate **500**. The passivation layer **560** is preferably made of SiO_2, but not limited thereto. The passivation layer **560** is patterned to form a via hole **565**. The via hole **565** exposes either the source or the drain electrodes **554** and **555**. In **FIG.** 8B, the via hole **565** exposes a portion of the drain electrode **555**.

[**0105**] A transparent conductive layer is deposited on the passivation layer **560** to a thickness of 200 nm using a sputtering technique and dry-etched to form a pixel electrode **570** as an anode electrode. The pixel electrode **570** is preferably made of a transparent conductive material such as indium tin oxide (ITO) or indium zinc oxide (IZO), but not limited thereto. The pixel electrode **570** is electrically connected to the drain electrode **555** through the via hole **565**.

[**0106**] Subsequently, a planarization layer **580** is formed on the passivation layer **560** and covers an edge portion of the pixel electrode **570** to expose a portion of the pixel electrode **570**, thereby forming an opening portion **585** on the pixel electrode **570**. In other words, an insulating layer made of acryl is deposited on the passivation layer **560** to a thickness of 350 nm at a speed of 1300 rpm using a spin-coating technique and patterned to define the opening portion **585**. Thereafter, the insulating layer is baked at a temperature of 220° C., thereby forming the insulating layer **580** in which a taper angle of an edge portion thereof is 15° and a thickness d**5** of a portion of the insulating layer formed on an edge of the pixel electrode **570** is less than 250 nm.

[**0107**] Referring to **FIGS. 8C and 8D**, an organic EL layer **590** is formed on the exposed portion of the pixel electrode **570** to cover an edge portion of the planarization layer **580** using a laser transfer technique.

[**0108**] In more detail, a PEDOT is spin-coated to a thickness of 50 nm at a speed of 3000 rpm and heat-treated at a temperature of 200° C. during five minutes to thereby form a hole transport layer **590***a*. Subsequently, three pieces of transfer films are manufactured. For the sake of description convenience, a method of manufacturing one transfer film **50** for an R color pattern is described.

[**0109**] The transfer film **50** for the R color pattern is manufactured as follows: on a base film **51** having a transfer layer **52** formed thereon, an R color organic electroluminescent material is spin-coated to a thickness of 80 nm at a speed of 2000 rpm using a xylene solution having a concentration of 1.0 wt/V %.

[**0110**] After aligning the transfer film **50** with the array substrate, the transfer film **50** is scanned by an infrared-rays laser so that a desired pattern is transferred to the hole transport layer **590***a,* thereby forming the R color pattern **590***b* of the organic EL layer. In the same method, G and B color patterns are formed to complete the organic EL layer **590**. The organic EL layer **590** can further include a hole injection layer, an electron transport layer and an electron injection layer.

[**0111**] A cathode electrode **595** is formed on the planarization layer **580** and covers the organic EL layer **590**. Preferably, the cathode electrode **595** has a dual-layered structure of Ca/Ag. Preferably, the Ca layer and the Ag layer have a thickness of 30 nm and 270 nm, respectively.

[**0112**] Finally, an encapsulation process is performed to complete the organic EL display device.

[**0113**] The methods of manufacturing the organic EL display device described above can be applied to those of **FIGS. 4 and 6**.

[**0114**] **FIG. 9** is a photograph illustrating the organic EL layer of the conventional organic EL display device of **FIG.** 1. As can be seen in **FIG. 9**, when a thickness of a portion of the insulating layer **180** corresponding to an edge of the pixel electrode **170** is more than 500 nm, the organic EL layer has defects F. That is, the organic EL layer is separated from the pixel electrode **170** or a boundary of the organic EL layer is not formed clearly.

[**0115**] **FIG. 10** is a photograph illustrating the organic EL layer of the organic EL display device according to the present invention. As can be seen in **FIG. 10**, when a thickness of a portion of the insulating layer corresponding to an edge of the pixel electrode is less than 500 nm, the organic EL layer has no defects. That is, the organic EL layer having a stable color pattern can be achieved.

[**0116**] For the laser transfer process, the transfer film having a thickness 50 nm to 100 nm is in contact with the array substrate. However, a step difference between the insulating layer and the pixel electrode is relatively great, for example, more than 500 nm, and the transfer film is not in contact with the array substrate. Therefore, the color pattern is unstably transferred to the array substrate, leading to defects of the organic EL layer. In the present invention, the insulating layer is formed to make the step difference between the insulating layer and the pixel electrode to be relatively low, i.e., less than 500 nm, so as to prevent the defect.

[**0117**] Meanwhile, the insulating layer is generally formed to a thickness of more than 1 μm to prevent a parasitic capacitor which may occur between the pixel electrode and the cathode electrode. However, even though the insulating layer is formed to a thickness of less than 500 nm, the parasitic capacitor does not occur.

[**0118**] The present invention can be applied to the active matrix organic EL display devices having two or more TFTs in a sub-pixel employing the organic EL layer having R, G and B color pattern and can also be applied to display devices having a partition wall between color patterns and using the laser transfer technique.

[**0119**] As described herein before, when a thickness of a portion of the insulating layer corresponding to an edge of the pixel electrode is less than 500 nm, it is possible to prevent defects of the organic EL layer in a boundary between the insulating layer and the pixel electrode, and a clean color pattern of the organic EL layer can be formed.

[**0120**] Although a few preferred embodiments of the present invention have been shown and described, it will be appreciated by those skilled in the art that changes may be made in these embodiments without departing from the principles and spirit of the invention, the scope of which is defined in the claims and the equivalents.

What is claimed is:

1. A display device, comprising:

a substrate;

an underlying layer formed over the substrate;

an insulating layer formed over the substrate to expose the underlying layer; and

an organic EL layer formed on the exposed portion of the underlying layer,

wherein a thickness of the insulating layer is less than 500 nm.

2. The device according to claim 1, wherein the thickness of the insulating layer is less than 200 nm.

3. The device according to claim 1, wherein the thickness of the insulating layer is in a range between 10 nm and 500 nm.

4. The device according to claim 3, wherein the thickness of the insulating layer is in a range between 100 nm and 200 nm.

5. The device according to claim 1, wherein the insulating layer is formed to cover an edge of the underlying layer.

6. The device according to claim 5, wherein a portion of the insulating layer corresponding to the edge of the underlying layer has a thickness of less than 200 nm.

7. The device according to claim 5, wherein a portion of the insulating layer corresponding to an edge of the underlying layer has a thickness of 10 nm to 500 nm.

8. The device according to claim 5, wherein the portion of the insulating layer corresponding to the edge of the underlying layer has a thickness of 100 nm to 200 nm.

9. The device according to claim 1, wherein a step of the insulating layer to the underlying layer is less than 200 nm.

10. The device according to claim 1, wherein a step of the insulating layer to the underlying layer is in a range between 10 nm to 500 nm.

11. The device according to claim 10, wherein the step of the insulating layer to the underlying layer is in a range between 100 nm to 200 nm.

12. An organice EL display device, comprising:

a substrate;

a thin film transistor having source and drain electrodes formed over the substrate;

a lower electrode contacting one of the source and drain electrodes of the thin film transistor;

an insulating layer formed over the substrate to expose the lower electrode; and

an organic EL layer formed on the exposed portion of the lower electrode,

wherein a thickness of the insulating layer is less than 500 nm.

13. The device according to claim 12, wherein the thickness of the insulating layer is less than 200 nm.

14. The device according to claim 12, wherein the thickness of the insulating layer is in a range between 10 nm and 500 nm.

15. The device according to claim 14, wherein the thickness of the insulating layer is in a range between 100 nm and 200 nm.

16. The device according to claim 12, wherein the insulating layer is formed to cover an edge of the underlying layer.

17. The device according to claim 16, wherein a portion of the insulating layer corresponding to the edge of the underlying layer has a thickness of less than 200 nm.

18. The device according to claim 16, wherein the portion of the insulating layer corresponding to the edge of the underlying layer has a thickness of 10 nm to 500 nm.

19. The device according to claim 16, wherein the portion of the insulating layer corresponding to the edge of the underlying layer has a thickness of 100 nm to 200 nm.

20. The device according to claim 12, wherein a step of the insulating layer to the underlying layer is less than 200 nm.

21. The device according to claim 12, wherein a step of the insulating layer to the underlying layer is in a range between 10 nm to 500 nm.

22. The device according to claim 21, wherein the step of the insulating layer to the underlying layer is in a range between 100 nm to 200 nm.

23. A method of manufacturing a display device, comprising:

forming an underlying layer over a substrate;

forming an insulating layer over the substrate to expose the underlying layer; and

forming an organic EL layer on the exposed portion of the underlying layer,

wherein a thickness of the insulating layer is less than 500 nm.

24. The method according to claim 23, wherein the thickness of the insulating layer is less than 200 nm.

25. The method according to claim 23, wherein the thickness of the insulating layer is in a range between 10 nm and 500 nm.

26. The method according to claim 25, wherein the thickness of the insulating layer is in a range between 100 nm and 200 nm.

27. The method according to claim 23, further comprising, forming a thin film transistor having source and drain electrodes over the substrate before the forming of the underlying layer.

28. The method according to claim 24, wherein the underlying layer is a lower electrode connecting one of the source and drain electrodes of the thin film transistor.

29. The method according to claim 28, wherein a thickness of the insulating layer is less than 200 nm.

30. The method according to claim 28, wherein a thickness of the insulating layer is in a range between 10 nm and 500 nm.

31. The method according to claim 30, wherein the thickness of the insulating layer is in a range between 100 nm and 200 nm.

32. The method according to claim 23, wherein the organic EL layer is formed using a laser tranfer technique.

33. The method according to claim 23, wherein the insulating layer has a taper angle on an edge portion thereof of 15 degrees.

34. A method of manufacturing a display device, comprising:

forming a thin film transistor over a substrate;

forming a passivation layer over the thin film transistor;

forming a pixel electrode as an anode electrode over a portion of the passivation layer and connected to a source or a drain region;

forming a planarization layer on the passivation layer and the edges of the pixel electrode to expose the pixel electrode;

forming an organic EL layer on the planarization layer; and

forming a cathode electrode layer on the planarization layer and the organic EL layer;

wherein the planarization layer is formed to a predetermined depth such that the forming of the organic EL layer is uniform across the whole length thereof.

35. The method according to claim 34, wherein the planarization layer has a thickness of less than 500 nm.

36. The method according to claim 35, wherein a portion of the planarization layer corresponding to edges of the pixel electrode layer has a thickness between 10 and 500 nm.

37. The method according to claim 36, wherein the portion of the planarization layer corresponding to the edges of the pixel electrode layer has a thickness between 100 nm and 200 nm.

* * * * *

专利名称(译)	有机EL显示装置及其制造方法		
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摘要(译)

一种显示装置，包括形成在基板上的下层;在衬底上形成绝缘层以暴露下层;形成在下层的暴露部分上的有机EL层，其中绝缘层的厚度形成为预定厚度，以防止可能在暴露部分的边缘部分中出现的有机EL层中的缺陷。